Docket No.: M4065.0951/P951-A

ABSTRACT

A CAM device architecture where CAM cells are divided into at least two arrays and each array is operated in a different clock domain so that at no time are the arrays simultaneously drawing maximum power. By dividing the CAM array into a plurality of arrays and staggering the search operation so that every array does not simultaneously draw maximum power, the peak power consumption of the CAM device is reduced.